

ABSTRACT

An integrated memory contains a memory cell array, which has word lines and bit lines, and a read/write amplifier, which is connected to the bit lines for the assessing and
5 amplifying data signals. A voltage generator circuit generates a voltage supply for application to the read/write amplifier. A potential difference is applied to the read/write amplifier using different supply potentials. The voltage generator circuit increases the potential difference applied to the read/write amplifier for a limited period of time during an assessment and amplification operation of the read/write amplifier. Charge-dependent
10 control is implemented in the voltage generator circuit. An assessment and amplification operation can be carried out at a comparatively high switching speed and a low power consumption is possible.